What is claimed is:

1. A method of testing a power amplifier and oscillator frequency in an integrated circuit based transmitter, said method comprising the steps of:

comparing a power amplifier output to a threshold and generating a square wave signal in response thereto, said threshold being adjusted such that said square wave signal is generated only when said power amplifier output voltage amplitude is above a predetermined level; and

dividing said square wave signal a sufficient number of times to enable frequency counting of a test output generated therefrom at a frequency significantly below that of said oscillator frequency.

2. The method according to claim 1, wherein said method is adapted to be implemented on-chip integral with said integrated circuit based transmitter.

3. The method according to claim 1, wherein a frequency count of zero or significantly below an expected level indicates a failure of said power amplifier to generate an acceptable output power level.

4. The method according to claim 1, wherein said threshold is dynamically configurable.

5. The method according to claim 1, wherein said predetermined level is set to screen said transmitter for compliance with a minimum power output level by said power amplifier.

6. The method according to claim 1, wherein said step of dividing comprises the step of dividing said square wave to a sufficiently low frequency to permit frequency counting using relatively low cost external test equipment.

7. The method according to claim 1, wherein said step of dividing comprises the step of dividing said square wave to a sufficiently low frequency thereby permitting frequency counting using existing on-chip processing means adapted to perform frequency counting.

8. The method according to claim 1, wherein said step of dividing comprises, for a 2.4 GHz oscillator frequency, the step of dividing said square wave by 128 to yield approximately a 19 MHz test output signal.

9. The method according to claim 1, wherein the division ratio for said square wave is divided is dynamically configurable.

10. The method according to claim 1, further comprising the step of applying said test output signal to a relatively low cost external frequency counter to verify compliance with a desired oscillator frequency.

11. The method according to claim 1, further comprising the step of applying said test output signal to an on-chip software/hardware based block adapted to verify compliance with a desired oscillator frequency range by means of frequency counting.

12. The method according to claim 1, wherein said oscillator frequency signal comprises carrier signal only.

13. The method according to claim 1, wherein said oscillator frequency signal comprises carrier signal combined with a modulating signal.

14. The method according to claim 1, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

15. The method according to claim 1, adapted to be implemented in a Field Programmable Gate Array (FPGA).

16. An apparatus for testing a power amplifier and oscillator frequency in an integrated circuit based transmitter, comprising:

means for comparing a power amplifier output to a threshold and generating a square wave signal in response thereto, said threshold being adjusted such that said square wave signal is generated only when said power amplifier output voltage amplitude is above a predetermined level; and

means for dividing said square wave signal a sufficient number of times so as to enable frequency counting of a test output generated therefrom at a frequency significantly below that of said oscillator frequency.

17. The apparatus according to claim 16, adapted to be implemented on-chip integral with said integrated circuit based transmitter.

18. The apparatus according to claim 16, wherein a frequency count of zero or significantly below an expected value indicates a failure of said power amplifier to generate an acceptable output power level.

19. The apparatus according to claim 16, wherein said threshold is dynamically configurable.

20. The apparatus according to claim 16, wherein said predetermined level is set to screen said transmitter for compliance with a minimum power output level by said power amplifier.

21. The apparatus according to claim 16, wherein said means for dividing is adapted to divide said square wave to a sufficiently low frequency to permit frequency counting using relatively low cost external test equipment.

22. The apparatus according to claim 16, wherein said means for dividing is adapted to divide said square wave, derived from a 2.4 GHz oscillator frequency, by 128 to yield approximately a 19 MHz test output signal.

23. The apparatus according to claim 16, wherein the division ratio by which the frequency of said square wave is divided is dynamically configurable.

24. The apparatus according to claim 16, further comprising means for applying said test output signal to a relatively low cost external frequency counter to verify compliance with a desired oscillator frequency.

25. The apparatus according to claim 16, wherein said oscillator frequency signal comprises carrier signal only.

26. The apparatus according to claim 16, wherein said oscillator frequency signal comprises carrier signal combined with a modulating signal.

27. The apparatus according to claim 16, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

28. The apparatus according to claim 16, adapted to be implemented in a Field Programmable Gate Array (FPGA).

29. An apparatus for testing a power amplifier and oscillator frequency in an integrated circuit based transmitter, comprising:

a comparator having a first input and a second input, wherein a power amplifier output signal is connected to said first input and a threshold signal is connected to said second input, said comparator operative to produce a square wave signal, wherein said threshold being adjusted such that said square wave signal is generated only when said power amplifier output voltage amplitude is above a predetermined level; and

a frequency divider adapted to receive the square wave signal output of said comparator and adapted to divide the frequency of said square wave to within a frequency range sufficiently below that of said oscillator frequency.

30. The apparatus according to claim 29, further comprising a configurable threshold register coupled to said second input of said comparator through a digital-to-analog converter, wherein said threshold register is adapted to be configurable via software or hardware means.

31. The apparatus according to claim 29, wherein said frequency divider is configurable and coupled to a configurable division register, wherein said division register is adapted to be configurable via software or hardware means.

32. The apparatus according to claim 29, adapted to be implemented on-chip integral with said integrated circuit based transmitter.

33. The apparatus according to claim 29, wherein a frequency count of zero indicates a failure of said power amplifier to generate an acceptable output power level.

34. The apparatus according to claim 29, wherein said threshold is dynamically configurable.

35. The apparatus according to claim 29, wherein said predetermined level is set to screen said transmitter for compliance with a minimum power output level by said power amplifier.

36. The apparatus according to claim 29, wherein said means for dividing is adapted to divide said square wave to a sufficiently low frequency to permit frequency counting using relatively low cost external test equipment.

37. The apparatus according to claim 29, wherein said means for dividing is adapted to divide said square wave to a sufficiently low frequency to permit frequency counting using internal processing means.

38. The apparatus according to claim 29, wherein said frequency divider is adapted to divide the frequency of said square wave to within a frequency range sufficiently below that of said oscillator frequency to enable frequency counting by on-chip processor means utilizing appropriate software adapted to execute on said processor means.

39. The apparatus according to claim 29, wherein said means for dividing is adapted to divide said square wave, derived from a 2.4 GHz oscillator frequency, by 128 to yield approximately a 19 MHz test output signal.

40. The apparatus according to claim 29, wherein the division ratio for said square wave is divided is dynamically configurable.

41. The apparatus according to claim 29, further comprising means for applying said test output signal to a relatively low cost external frequency counter to verify compliance with a desired oscillator frequency.

42. The apparatus according to claim 29, wherein said oscillator frequency signal comprises carrier signal only.

43. The apparatus according to claim 29, wherein said oscillator frequency signal comprises carrier signal combined with a modulating signal.

44. The apparatus according to claim 29, adapted to be implemented in an Application Specific Integrated Circuit (ASIC).

45. The apparatus according to claim 29, adapted to be implemented in a Field Programmable Gate Array (FPGA).